Project Report : EEE454 VLSI I Group No : 15

PROJECT TITLE: **VLSI Design of 4 bit ALU with Shifter using Cadence®**

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ABSTRACT

An arithmetic logic unit (ALU) is the fundamental block of digital electronic computing circuit that carries out arithmetic and bitwise logical operations on integer binary numbers. We were assigned to design a 4-bit ALU with shifter for this project using Cadence® Virtuoso schematic editor and Layout Suite L Editor. In this report we have demonstrated the process used to design the schematic of 4 bit Arithmetic Logic Unit (ALU) and a Shifter along with the layout of Shifter and Adder (used in the ALU) meeting the specifications given in the specification table. The whole design was sorted into several sub-circuits which were next built using only CMOS implementation. The final design was then formed by merging all sub- circuit components. Moreover layouts of the components were also prepared in accordance with the schematic. The layouts were both DRC and LVS error free
.

KEYWORDS:

1. ALU

2. ADDER

3. SHIFTER

4. DRC

5.Buffer

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INTRODUCTION

This project is about designing a 4 bit ALU which will implement 12 functions. Arithmetic and Logic Unit (ALU) represents the fundamental blocks of central processing unit in a modern computer architecture that performs all the arithmetic calculations and logical operations required by a program. Our earlier courses introduced us to the structure and design of ALU. However, this sessional course introduces us to designing real life integrated circuits using Cadence® which brings us to the endeavor of designing an ALU along with a 4-bit Shifter unit using Cadence.

This project present us with the challenge of not only designing the logic based design of ALU but also developing it into a VLSI design using creative decisions for optimization and conforming with all the Nano-scaled design rules (DRC), which ultimately developed a depth of knowledge about VLSI design on an intuitive and experimental basis.

THEORY

ALU is a combination of two separate functioning blocks, apparently, the arithmetic block and the bitwise logic block. These two block have to be separately or jointly accessible by the computer control system. The arithmetic unit deals with the addition/ subtraction operations whereas bitwise logic operations performs AND OR XOR etc. logical operations on the operands. The shifter unit then shifts the output bits in both direction (left/right) according to design specifications.

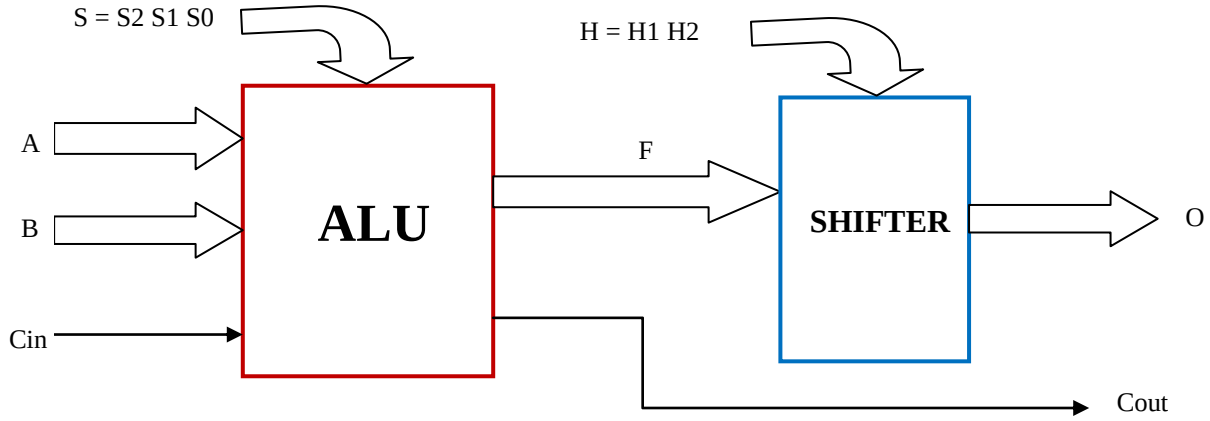

FIGURE 1: BLOCK DIAGRAM OF ALU WITH SHIFTER

We have been assigned the following tasks with their corresponding opcodes to implement in designing the ALU & Shifter.

TABLE 1: OPCODES AND OPERATIONS

Opcode (s2s1s0cin)	Operations		
	F	**Cout**	**Description**
0000	**A**	**1**	**TRANSFER A**
0001	**A+B+1**	**1 IF A+B ≥2^4 -1**	**Add B with A with A carry**
0010	**A-B-1**	**1 IF A>B**	**Subtract B From A With Borrow**
0011	**A+1**	**1 IF A= 2^4 -1**	**Increment A**
0100	**A**	**0**	**TRANSFER A**
0101	**A+B**	**1 IF A+B ≥2^4**	**Addition of A & B**
0110	**A-B**	**1 IF A≥B**	**Subtraction of A & B**
0111	**A-1**	**1 IF A≠0**	**Decrement A**
1001	**A'**	**0**	**COMPLEMENT A**
1011	**A or B**	**0**	**BITWISE OR**
1101	**A and B**	**0**	**'' AND**
1111	**A xor B**	**0**	**'' XOR**

H1	H2	OPERATION	FUNCTION
0	0	O=F	NO SHIFT
0	1	O=SHR(F)	1 BIT RIGHT
1	0	O=SHL(F)	1 BIT LEFT
1	1	O=0	TRANSFER 0

To implement the above operations we have divided the ALU in 2 units –

- **Arithmetic unit:** This unit **consists of AND gate, XOR gate and an ADDER.** The operand A is directly transmitted to the adder whereas the operand B passes through a buffer of AND & XOR as per the requirement of operation (opcodes 0000 -0111). This unit is controlled with S1 S0 Cin. There are some internal control unit producing the signals X,Y,Z for the operation of AND ,XOR & the first carry in for adder respectively. **The additional control signals X Y Z are function of S1S0 Cin** . The unit Z acts as the carry generator for the 4 bit ADDER unit. Hence it is used only once as the carry in bit for LSB adder. For the higher bit adders , Cout from previous addition was taken as Carry in.

- **Logic unit** :This unit **consists of the individual logic blocks(nor,nand, xnor) and a 4-1 mux.** Control signals for this unit are S1 & S0 which controls the 4-1 mux and select the logic operation at its input according to the command. 4-1 mux gives inverted output of the desired logic operation .so an inverter is placed after it.

The outputs from the above 2 unit are then fed into a 2-1 mux which is controlled with S2.All the blocks except SHIFTER are designed as unit cell for 1 bit operation of A and B. Later the unit cells had been replicated and merged to function as 4 bit ALU. Next, the output F from ALU is directly passed to a 4 bit SHIFTER where the outputs experience 1 bit left/right shift or no shift at all as per the command. The shifter is controlled with H1 H2. Finally after shifter a buffer unit is placed the to boost the output signals. All the blocks of sub-circuits have been built by CMOS implementation.

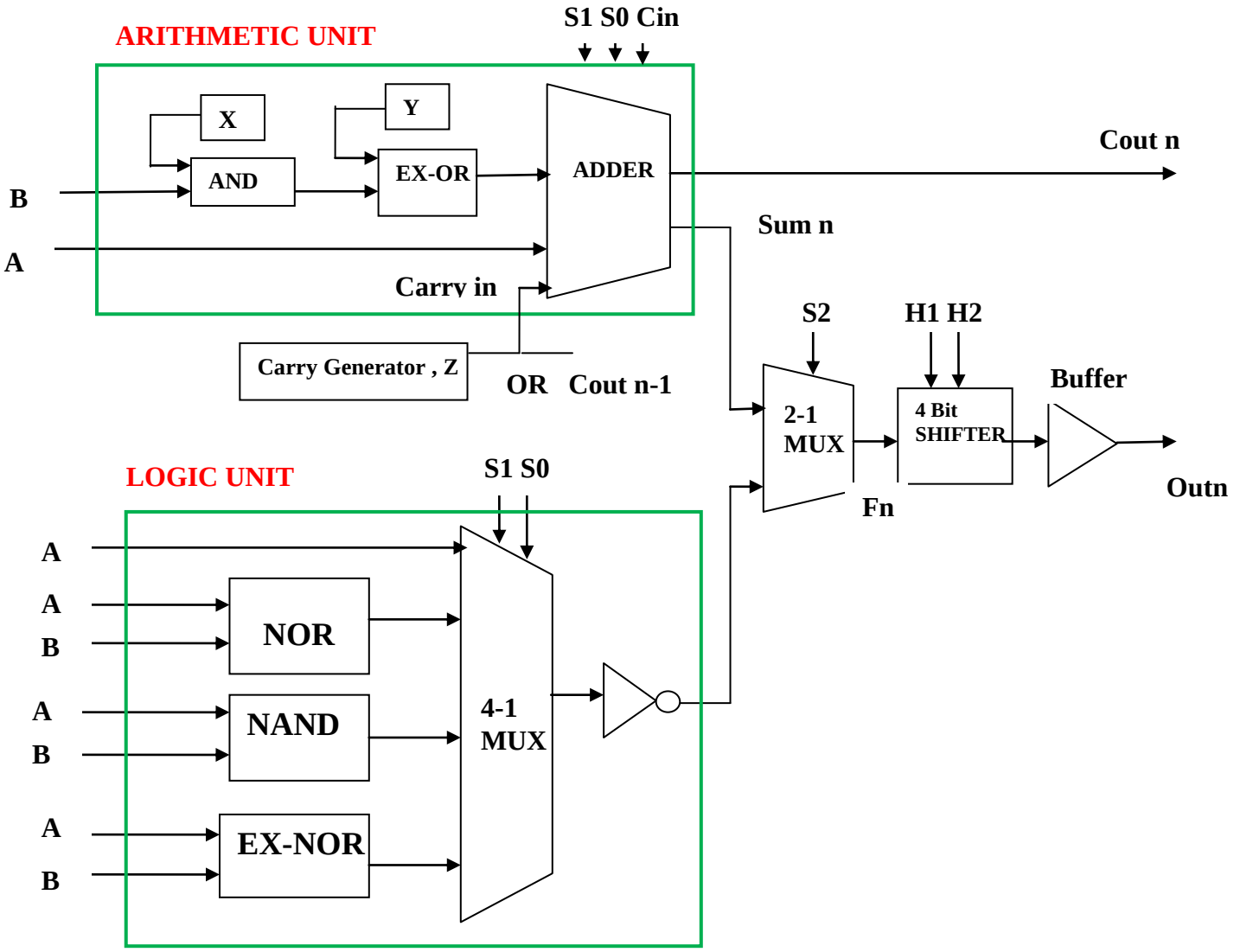

FIGURE 2 : BLOCK DIAGRAM STRUCTURE OF THE DESIGNED 4 BIT ALU WITH SHIFTER

The functions for additional control units X , Y, Z in Arithmetic block were derived using the following truth table

TABLE 2 : Truth Table for Internal control signals X, Y, Z

S_2	S_1	S_0	C_{in}	X	Y	Z
0	0	0	0	0	1	1
0	0	0	1	1	0	1
0	0	1	0	1	1	0
0	0	1	1	0	0	1
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	1	1	1

0	1	1	1	0	1	0
1	0	0	1	D	D	D
1	0	1	1	D	D	D
1	1	0	1	D	D	D
1	1	1	1	D	D	D

By solving K-map , we derived the following functions-

X= S0 $\overline{Cin}$ + $\overline{S0}$ Cin

Y= S1 S0 +$\overline{S1}$ $\overline{Cin}$

Z= $\overline{S1}$ Cin + $\overline{S1}$ $\overline{S0}$ + S1 S0 $\overline{Cin}$

TOOLS USED

- Cadence® Virtuoso Schematic L Editor
- Cadence® Virtuoso Layout Suite XL Editor

PROCEDURE

1. First to make the design process less complicated, the sub-circuits blocks of arithmetic and logic unit were created individually using schematic XL. The blocks were simulated to verify their functionality before merging in the combined design. The designs were initially generated for 1 bit operands.

2. Next the Arithmetic unit and Logic unit were formed merging their component circuitry and a symbol were formed for each unit.

3. Additional circuits like Carry generator Z, 2-1 mux, 4 bit shifter, Inverters were also formed and a symbol was generated for each.

4. Finally all the units were replicated and combined to form the 4 bit ALU with shifter.

5. The control signal buses (H1 H2 S2 S1 S0 Cin) have been made available as both true and complimentary forms in the final combined circuit. This approach minimized the number of inverting transistors.

6. The schematic of 4 BIT ALU was simulated with Analog Design Environment (ADEL) and thus its functionality was verified.

7. Next the layouts were generated from the individual schematics of sub-circuits using virtuoso XL Layout Suite. The layouts of 4-1 mux were replicated 4 times and merged to form the SHIFTER layout. Same process was followed for designing the layout of ADDER unit. The layouts were DRC and LVS verified.

RESULTS

The cmos circuit design for each sub-circuits and their corresponding symbols and Layouts are given-

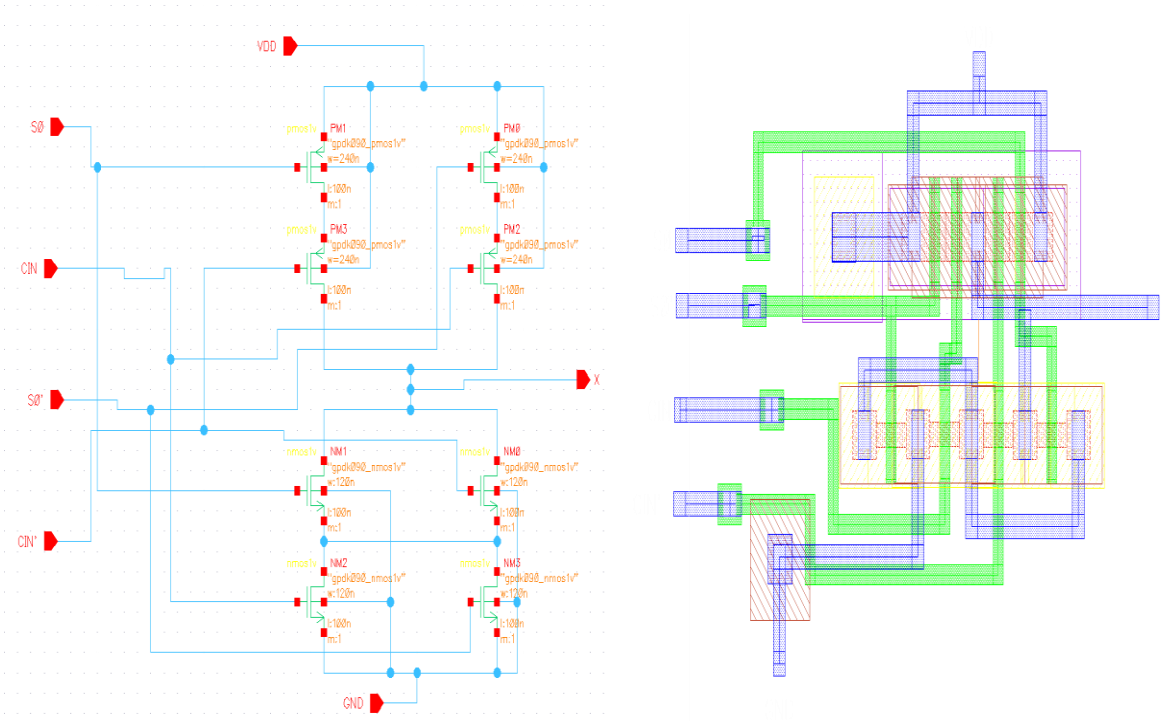

FIGURE 3: SCHEMATIC AND LAYOUT OF SUB-CIRCUIT X

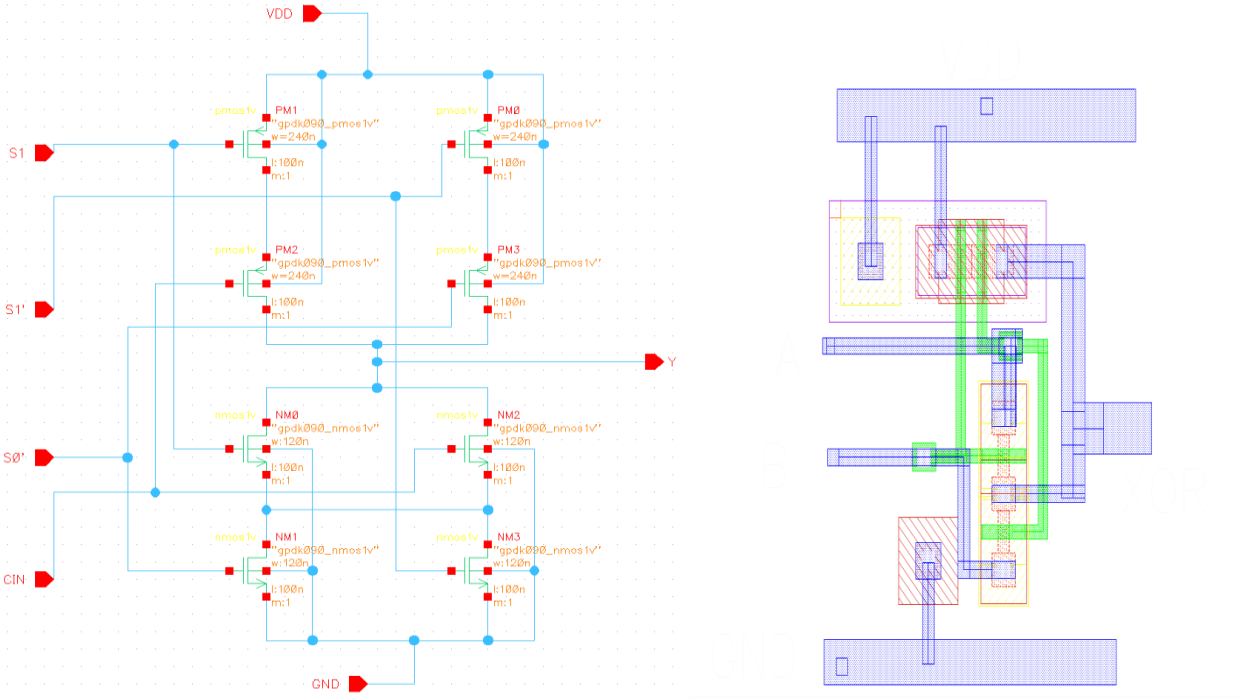

FIGURE 4: SCHEMATIC AND LAYOUT OF SUB-CIRCUIT Y

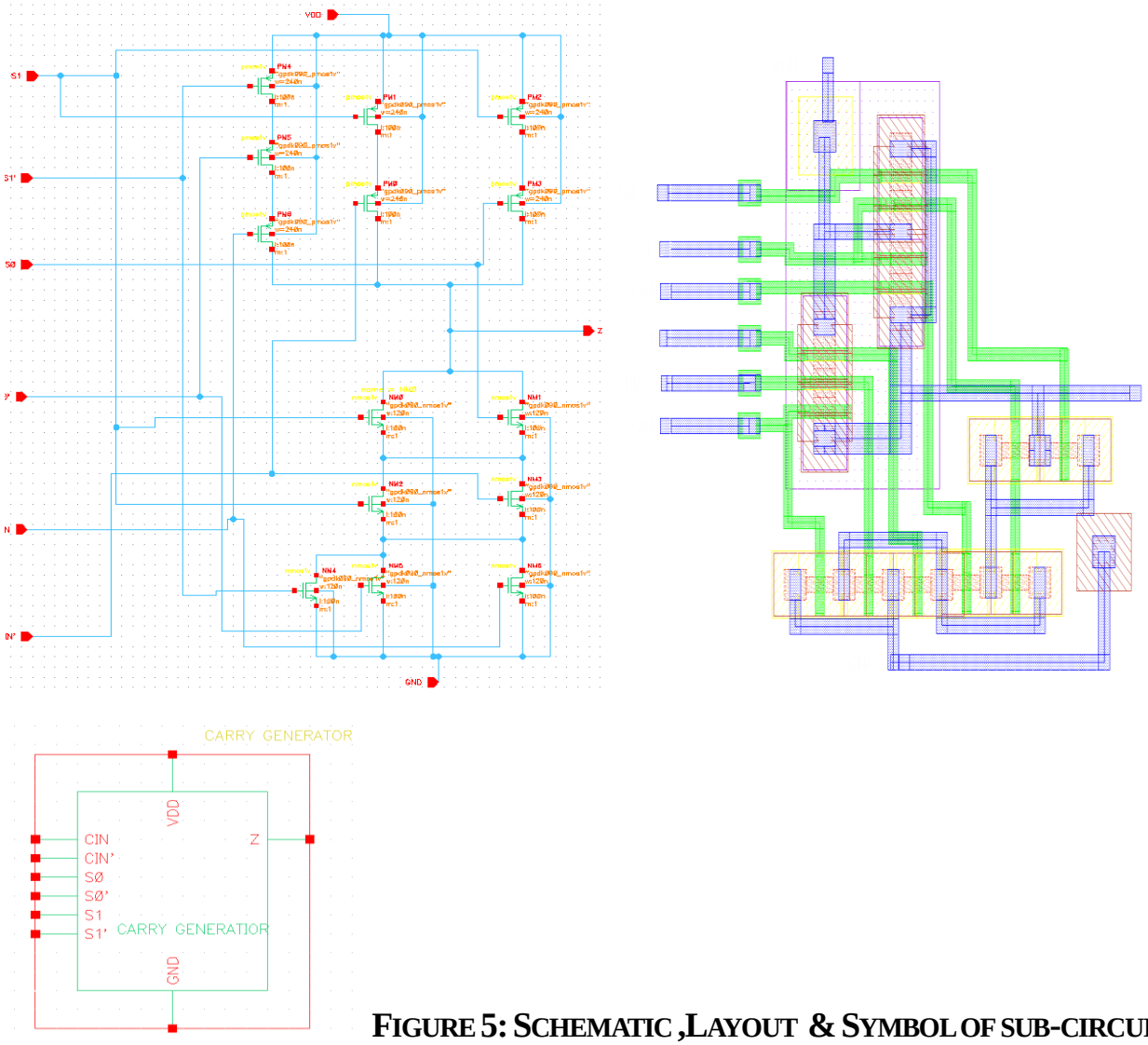

FIGURE 5: SCHEMATIC ,LAYOUT & SYMBOL OF SUB-CIRCUIT Z

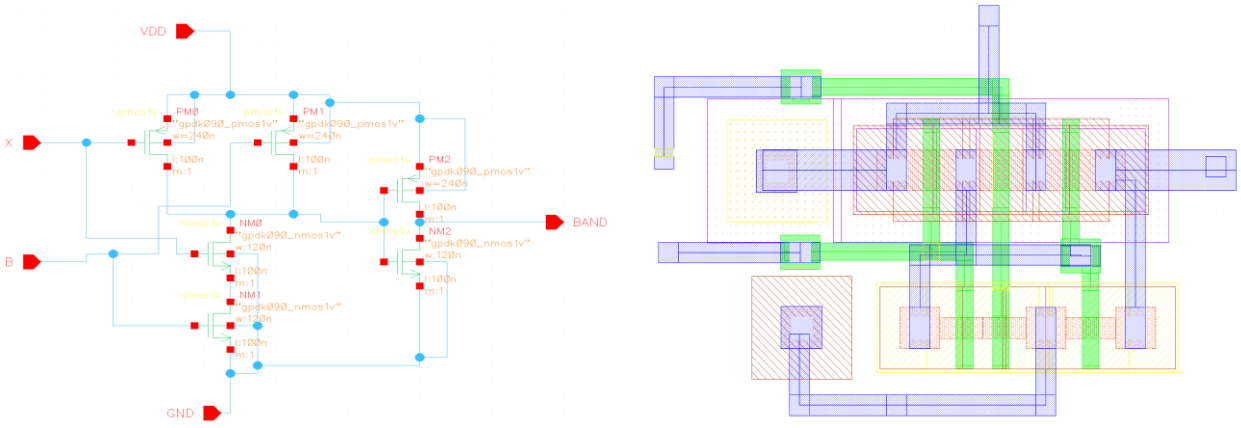

FIGURE 6: SCHEMATIC AND LAYOUT OF SUB-CIRCUIT AND IN ARITHMETIC UNIT.

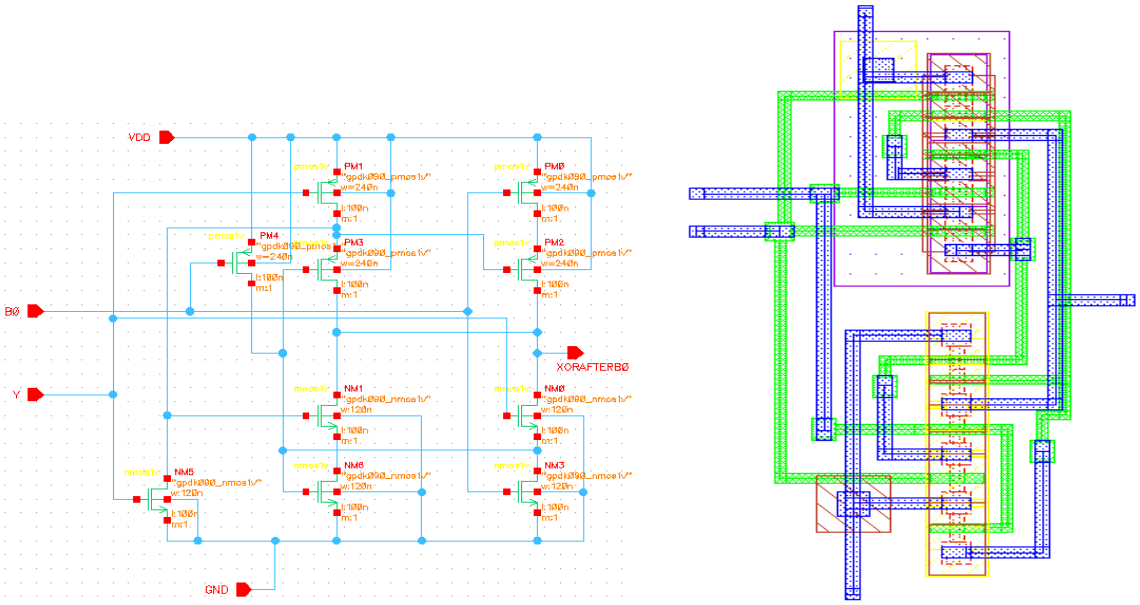

FIGURE 7: SCHEMATIC AND LAYOUT OF SUB-CIRCUIT XOR IN ARITHMETIC UNIT.

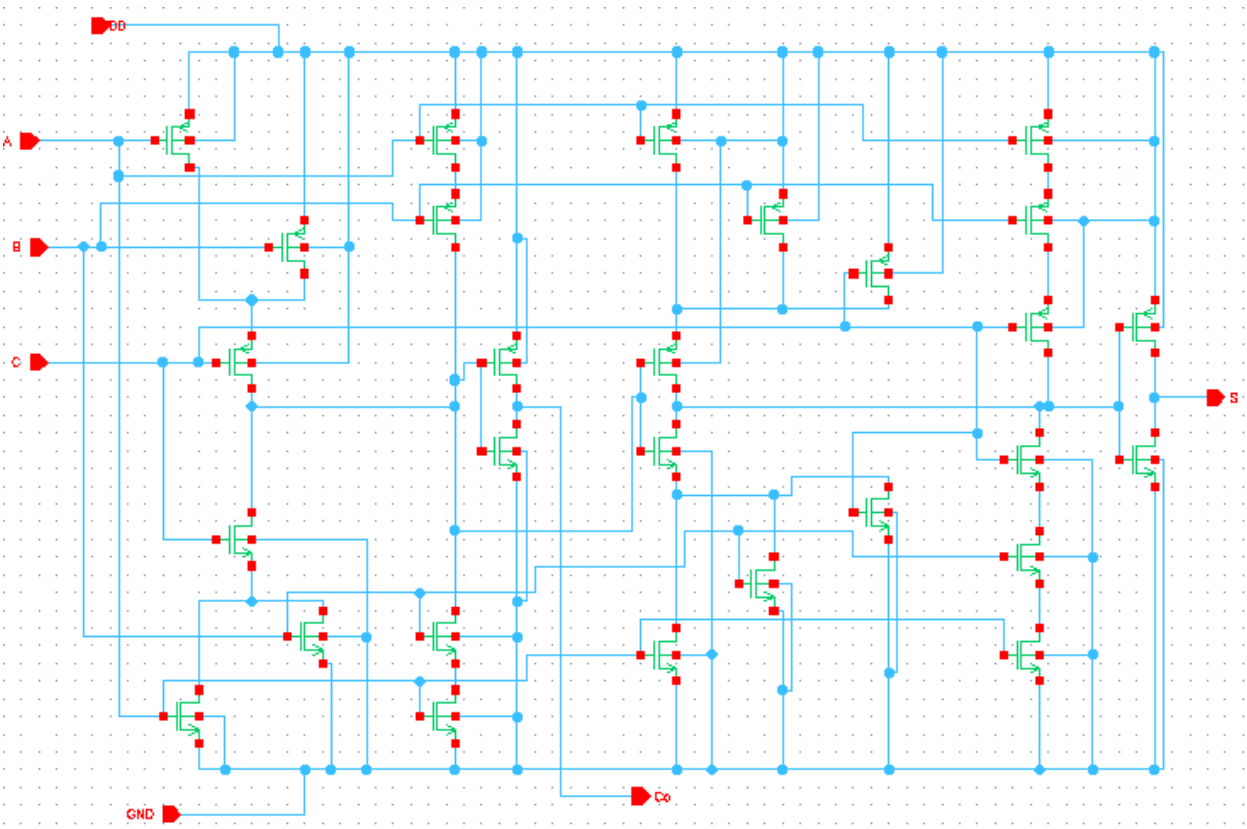

FIGURE 8: SCHEMATIC OF 1 BIT ADDER.

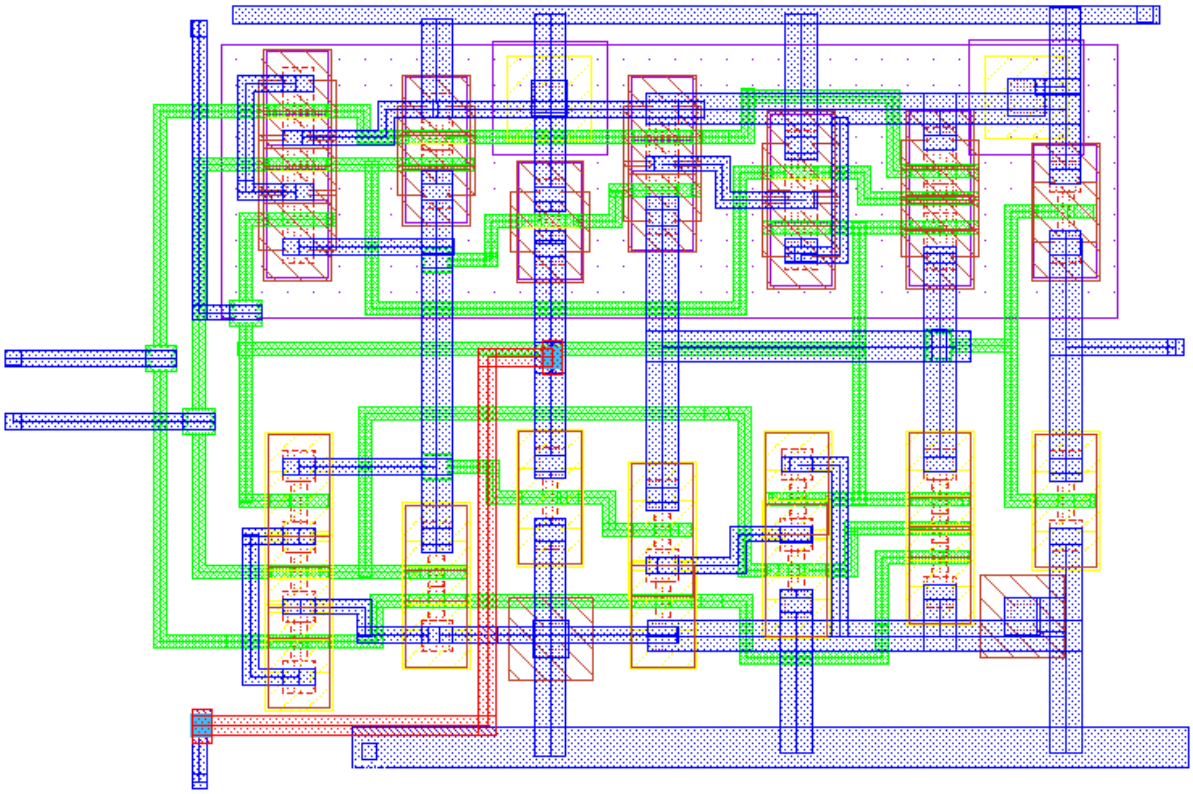

FIGURE 9: LAYOUT OF 1 BIT ADDER.

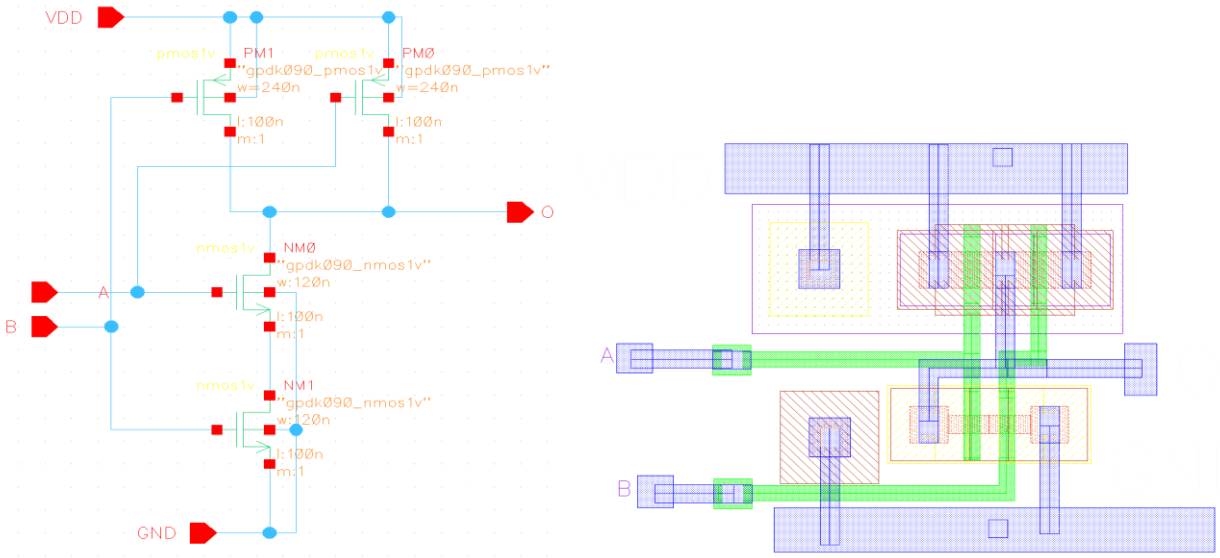

FIGURE 10: SCHEMATIC AND LAYOUT OF NAND IN LOGIC UNIT.

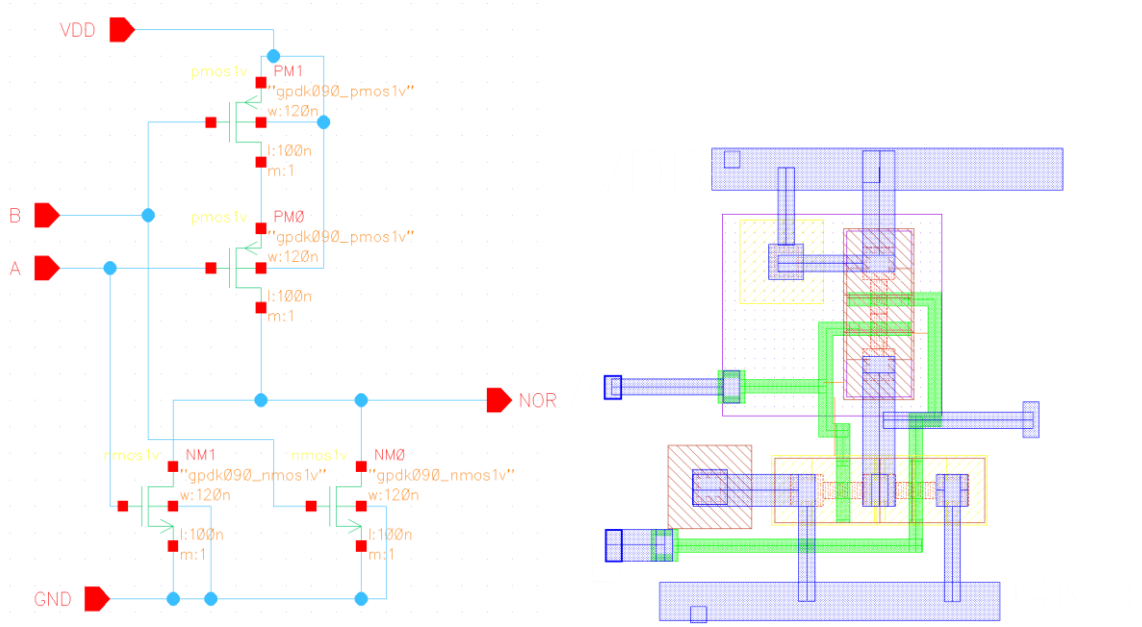

FIGURE 11: SCHEMATIC AND LAYOUT OF NOR IN LOGIC UNIT

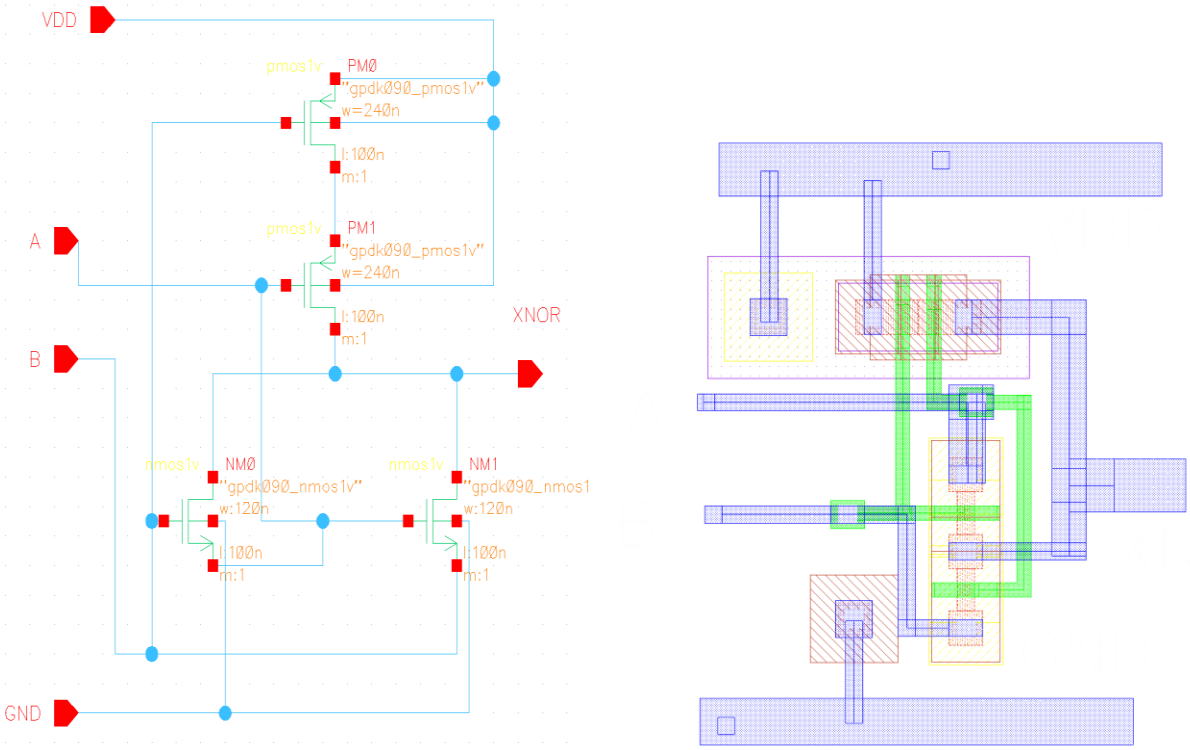

FIGURE 12: SCHEMATIC AND LAYOUT OF XNOR IN LOGIC UNIT

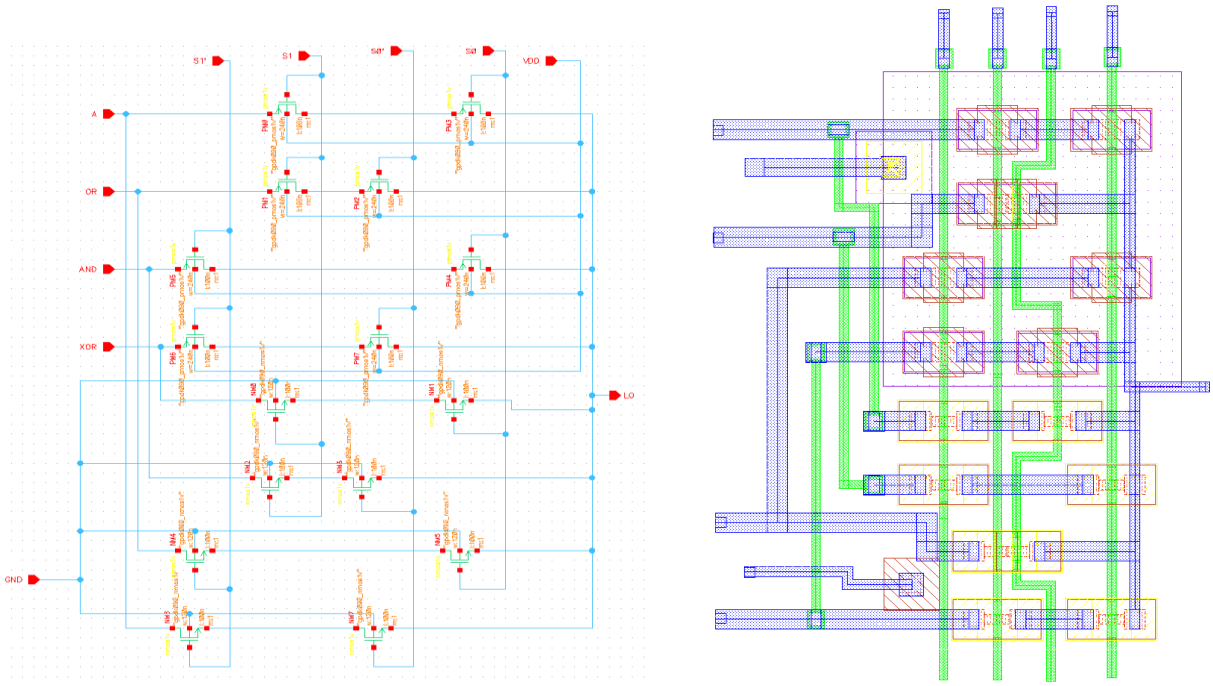

FIGURE 13: SCHEMATIC AND LAYOUT OF 4-1 MUX USED IN ARITHMETIC UNIT

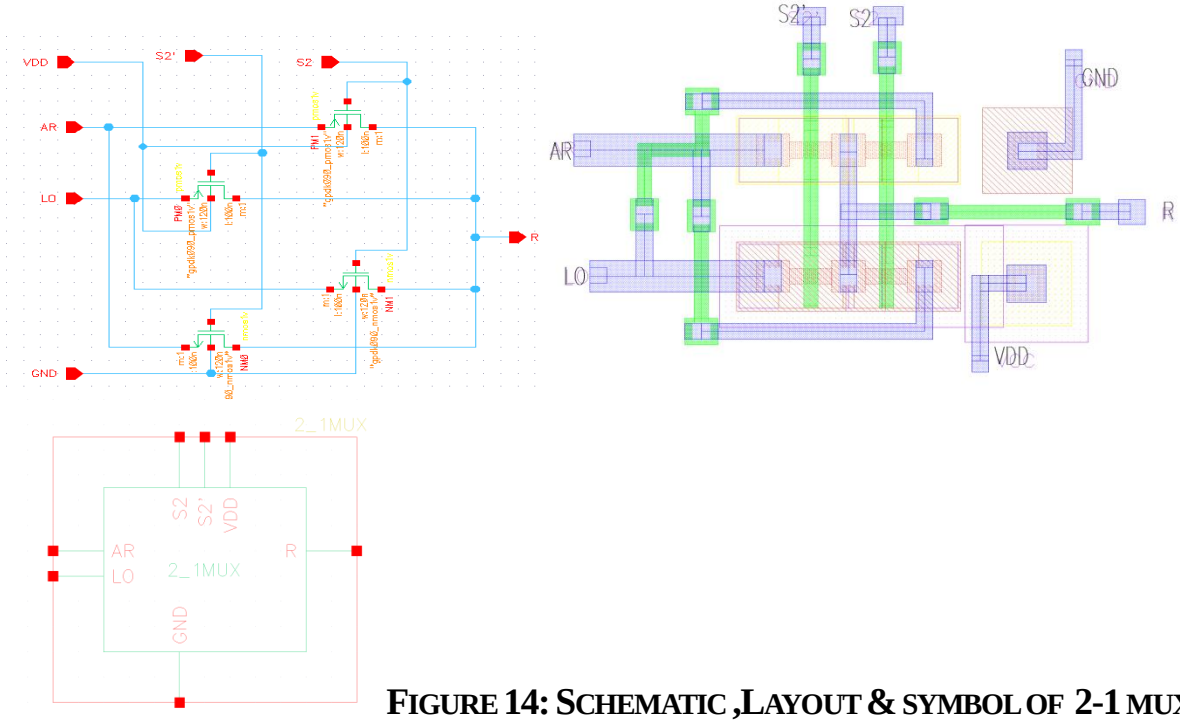

FIGURE 14: SCHEMATIC ,LAYOUT & SYMBOL OF 2-1 MUX

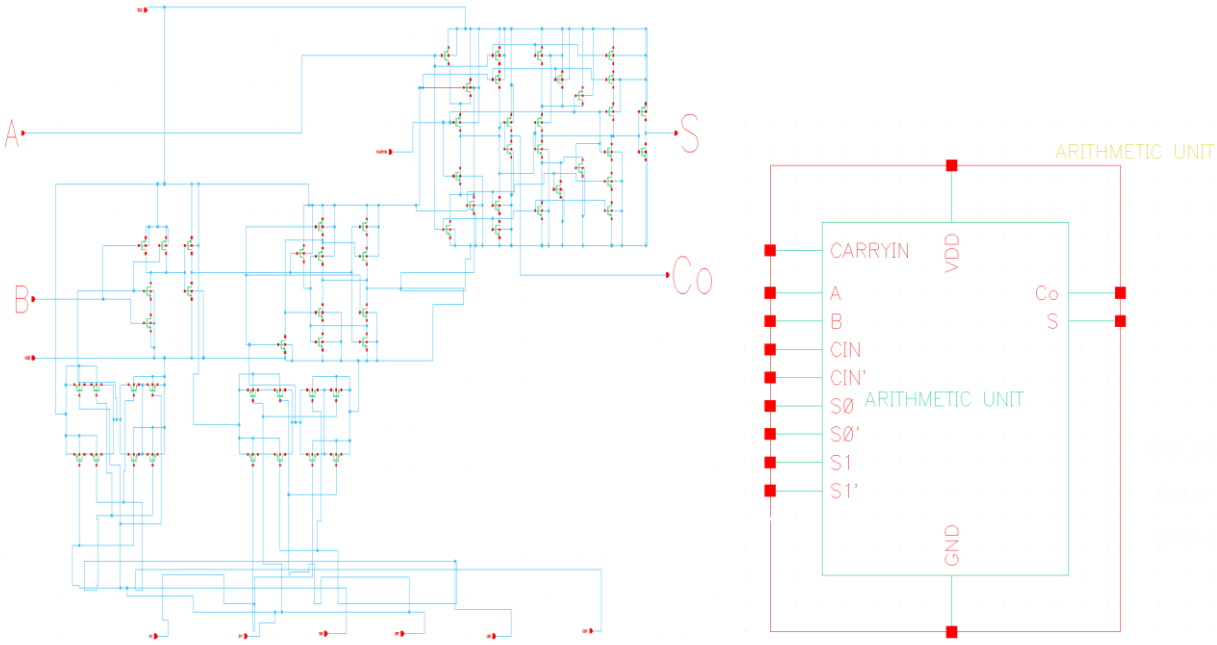

FIGURE 15: SCHEMATIC & SYMBOL OF ARITHMETIC UNIT

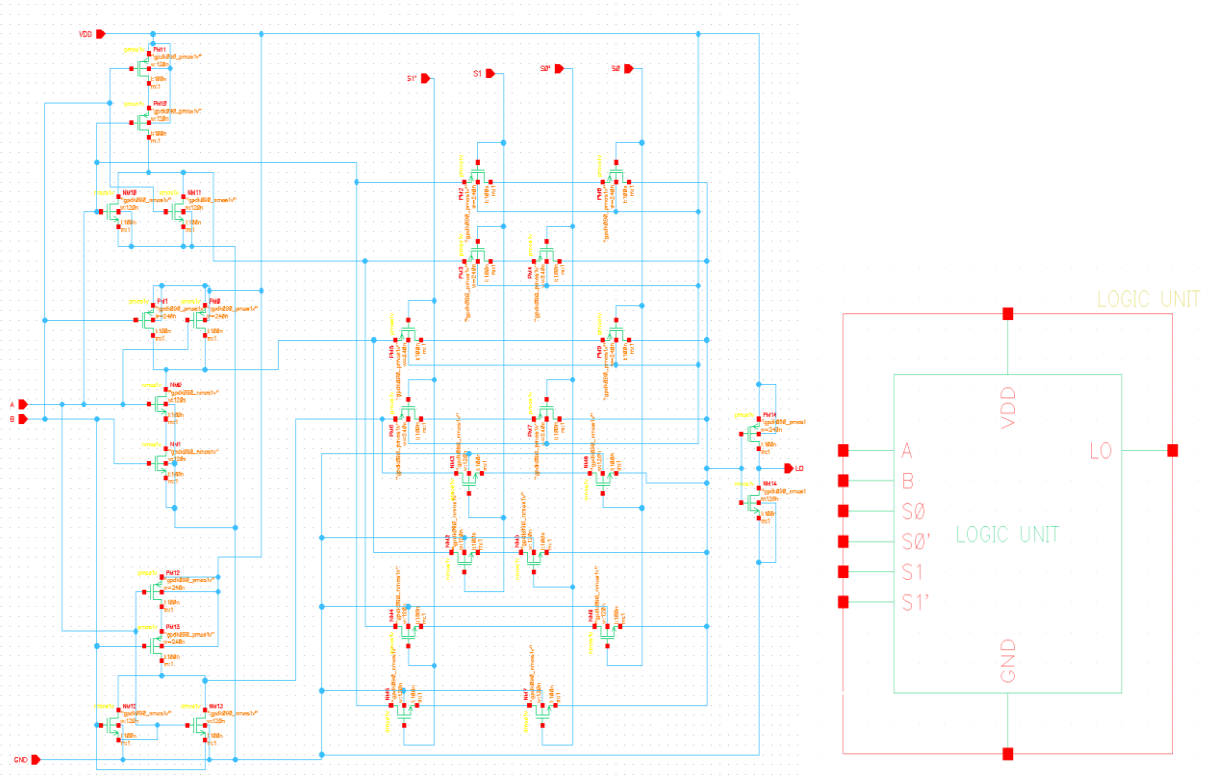

FIGURE 16: SCHEMATIC & SYMBOL OF LOGIC UNIT

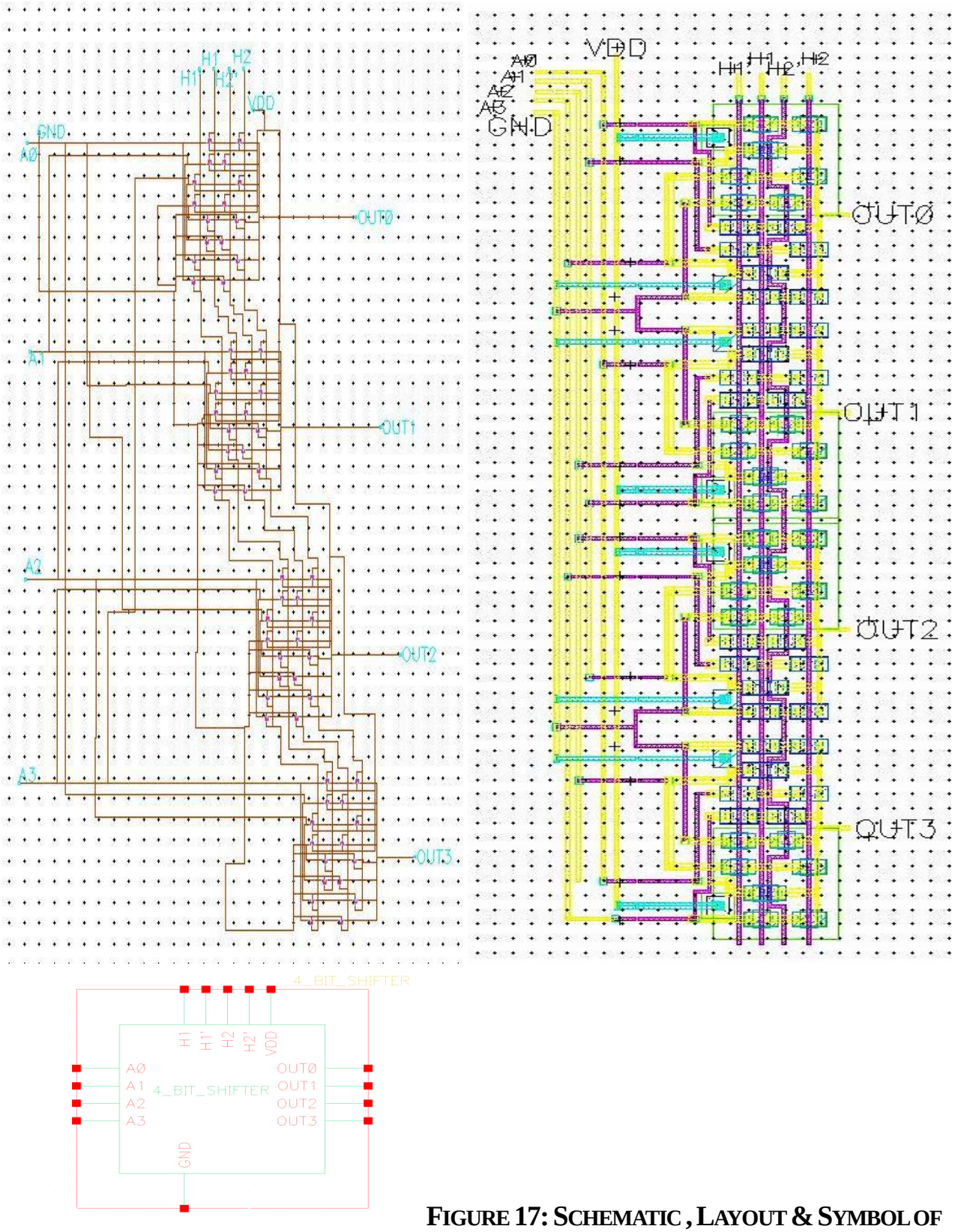

FIGURE 17: SCHEMATIC , LAYOUT & SYMBOL OF SHIFTER

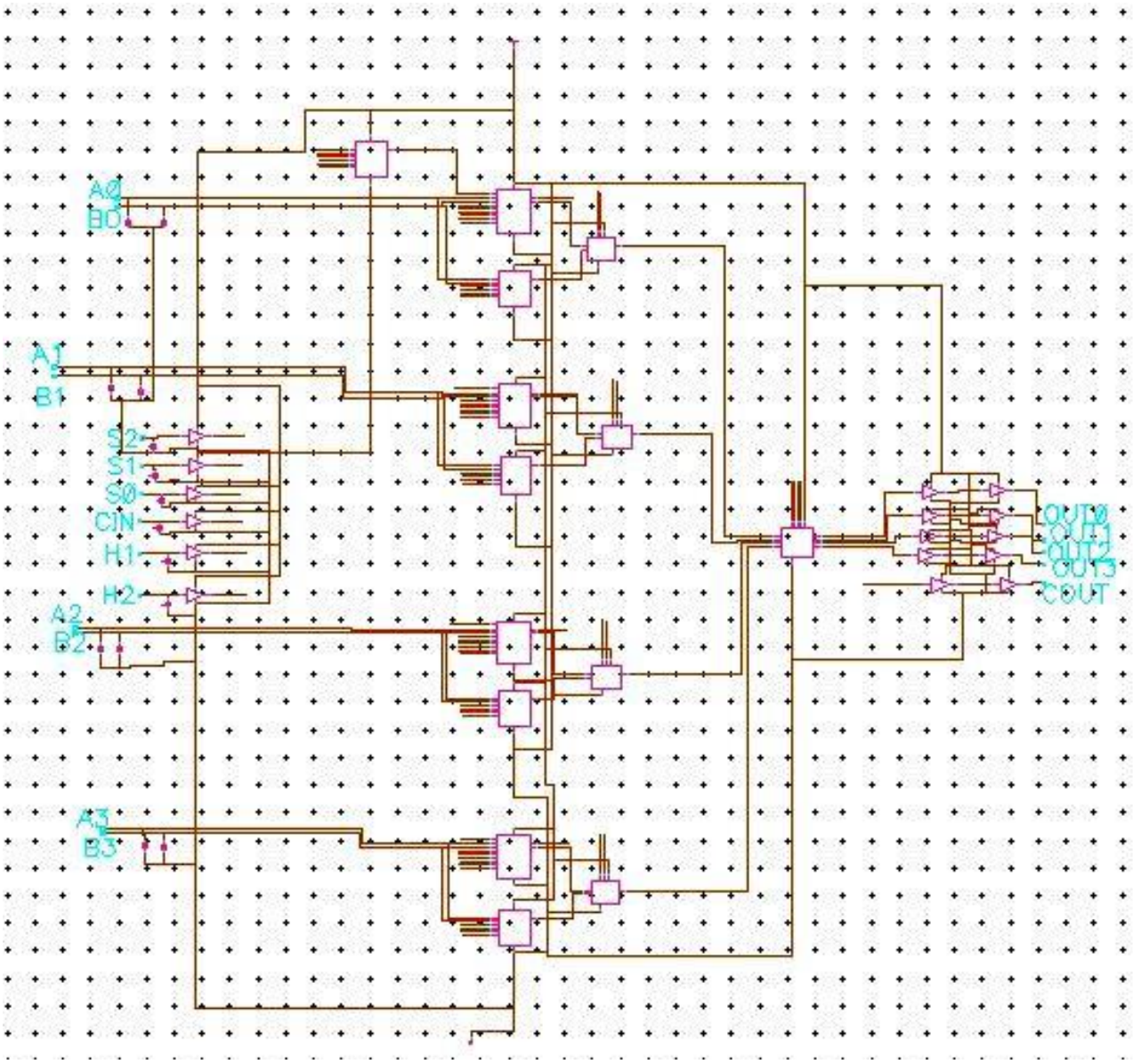

FIGURE 18: SCHEMATIC OF 4 BIT ALU WITH SHIFTER.

A sample simulation in ADEL was performed for A= 1010 & B=0011. We can observe the output values before and after shifter operation for the opcode H1H2S2S1S0Cin = 100110 in the timing diagram. From Table1 we find the operation to be A – B with one bit left shift. The timing diagram of the observed output is shown below-

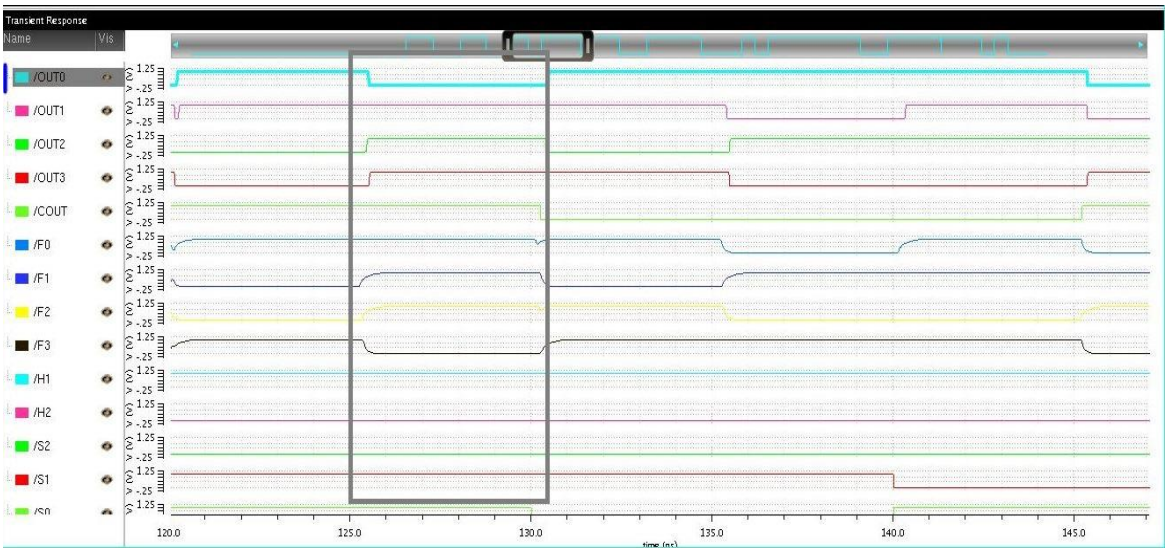

FIGURE 19: TIMING DIAGRAM FOR A-B WITH 1 BIT LEFT SHIFT (A= 1010 & B= 0011)

The numbers of transistors, used in the whole design are also noted down in the following tables. Moreover the cell area of the layout has also been calculated and recorded.

TABLE 3: Number of TRANSISTORS used in the Design

Circuit Block Name	Single Bit Circuit		4 Bit Circuit	
	NMOS	PMOS	NMOS	PMOS
Arithmetic Unit				
X	4	4	16	16
Y	4	4	16	16
Z			7	7
ADDER	14	14	56	56
AND	3	3	12	12
XOR	5	5	20	20
Logic Unit				
NAND	2	2	8	8
NOR	2	2	8	8
XNOR	2	2	8	8
4-1 MUX	8	8	32	32
Inverter	1	1	4	4
2-1 MUX	4	4	16	16
4-bit Shifter			32	32
Buffer			10	10
Complementary selectors			6	6
TOTAL	**49**	**49**	**251**	**251**

TABLE 4: Cell view areas of the sub-circuits used in the Design

Circuit Block Name	Layout size (µm X µm	Area (μm^2)
X	4.5X2.8	12.6
Y	3.3X3.8	12.54
Z	4.4X4.5	19.8
1 bit ADDER	8.33X5.8	48.314
NAND	2.83X2.36	6.67
NOR	2.74X3.4	9.316
XNOR	3.3X3.7	12.21
4-1 MUX	5.09X706	38.684
SHIFTER	9.26X30.14	279.096

CONCLUSION

Cadence Virtuoso® Schematic and Layout Editor has made the task designing and implementing logic circuits easier and efficient. This project is a step towards finding efficient way of designing ALU and Shifter with less transistors and small IC size keeping the related design rules in mind. The layout of this project which we performed might not be the smallest design but our approach was to minimize the transistor numbers and complexities of the circuits as much as possible in spite of our design constraints.

REFERENCES

1. M. Morris Mano, “Digital Logic and Computer Design” , Second Edition.
2. Douglas A. Pucknell, Basic VLSI Design, Third Edition.