# Khan Shaikhul Hadi

shaikhulhadi@ucf.edu | github.com/shaikhulhadi | shaikhulhadi.github.io | linkedin.com/in/shaikhulhadi

## EDUCATION

**PhD** in **Computer Science** | University of Central Florida (UCF) *Expected graduation: Dec 2026*

- ***Research**: Addressing performance, correctness & crash consistency challenges of persistent parallel programming in fabric-attached persistent memory system; simulating and validating designs in gem5 (≈500,000 line open-source multi-core simulator).*
- *Awarded UCF Faculty Cluster Initiative (FCI) Student **Scholarship** 2025 ($5,000).*

**M.Sc.** in **Computer Science** | University of Central Florida (UCF) ***CGPA 3.9/4***

- *Relevant Coursework: **Advanced & Parallel Computer Architecture**, Machine Learning, Design & Analysis of Algorithms*

**B.Sc.** in **Electrical Engineering** | Bangladesh University of Engineering and Technology (BUET) ***CGPA 3.43/4***

- *Relevant Coursework: Microprocessor and Interfacing, VLSI `I` & `II`, Digital Circuit Design*

## RELEVANT EXPERIENCE

**Graduate Research Assistant** | ARPERS Research Group, UCF *Jan 2021 - Jul 2025*

- *Developed cycle-level simulation model for CXL switch with CXL.mem (Type-3) and port-based routing (PBR) support (Authored ≈**22,000 lines of C++ & Python** code) for switch-level **performance and behavior analysis**. Designed data persistence support at switch-level that ensured crash consistency and data correctness; achieved an **average 15% speedup** on evaluated benchmark.*
- *Extended Sniper multi-core simulator with a memory access contention model and transient-state changes at cache coherence model for shared memory access, enabling evaluation that resulted in publication.*

**Graduate Teaching Assistant** | School of Engineering, UCF *Aug 2022 - Dec 2022, Aug 2025 - Present*

- *Counseled students to understand complex topics like cache coherence & organization in **Advanced & Parallel Computer Architecture**; delivered **guest lectures** on cache; mentored and evaluated **C++**/Java cache design projects.*

**Research Engineer** | BUET-Energypac Research Collaboration *Apr 2017 - Oct 2018*

- *Designed and characterized TSMC 180 nm BUET Standard Cell Library (50 digital, 3 analog). Applied Cadence tools & TCL automation to streamline **ASIC** design flows*
- *Prototyped an LED driver controller IC in **Verilog** and completed **RTL** synthesis, DRC, and LVS in the Cadence Design Suite with the integrated standard cell library. This achieved a successful first-spin fabrication through EUROPRACTICE IC Service in June 2018.*

## SELECTED PROJECTS *(Full List )*

**Durable Atomics Instructions** ***Published in DAC 2023***

- *Engineered durable atomic instructions support via transient states of **cache coherence** protocol to achieve crash consistency for parallel programming in persistent memory system.*
- *Accomplished the primary goal of crash consistency and also realized **6.4% average speedup** on SPLASH-4 benchmark; simulated in Sniper Multi-Core Simulator which led to a publication & nomination to present at the Non-Volatile Memory Workshop (**NVMW**) 2024.*

**Bare-Metal Operating System**

- *Wrote a from-scratch, bare-metal operating system in **C**, produced a bootable image, and validated functionality in QEMU.*
- *Implemented core kernel features, including a **bootloader** to load the kernel, an **interrupt-handling** protocol, a keyboard driver, and a basic video driver for terminal output.*

**Specialized SAP microprocessor**

- *Architected an **8-bit register microprocessor** with single-bus architecture, 64KB memory and 16-instruction ISA (including PUSH/POP) using Proteus Design Suite. Optimized usage of temporary register count by leveraging idle IR as temporary register.*
- *Built a C++ based compiler to translate **assembly** to binary in hexadecimal format for program loading.*

**Sentiment analysis of stocks from financial-news headlines with Twitter feedback**

- *Built an NLP pipeline: scraped headlines (**Python/BeautifulSoup**), retrieved tweets (snscrape), normalized text, extracted nouns, and scored sentiment with **NLTK**; Programmed aggregation by remapping scores and using geometric means to curb outliers.*
- *Fused headline and tweet signals into one tunable feature. Performed **sensitivity studies** on large-cap tech tickers; plotted mismatches and documented research limits (headline misdirection, missing joint datasets, tweet reach/timing).*

## SELECTED PUBLICATION *(Full List )*

- ***Khan Shaikhul Hadi**, Naveel-ul Mustafa, Mark Heinrich & Yan Solihin, **"Hardware Support for Durable Atomic Instructions for Persistent Parallel Programming"**, Design Automation Conference (DAC), 2023*

## RELEVANT SKILLS

**Programming Languages**: *C/C++ (proficient), Python (proficient), OpenMP, Bash scripting, Verilog, TCL*
**Architecture Simulation Tool**: *gem5 Simulator, Sniper Multi-Core Simulator*